Nanosecond Risetime Pulse Characterization of SiC p^+n Junction Diode Breakdown and Switching Properties

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Outline

Pulse testing reveals very important SiC device behaviors not observed by conventional DC and RF testing.

Reverse bias diode pulse testing

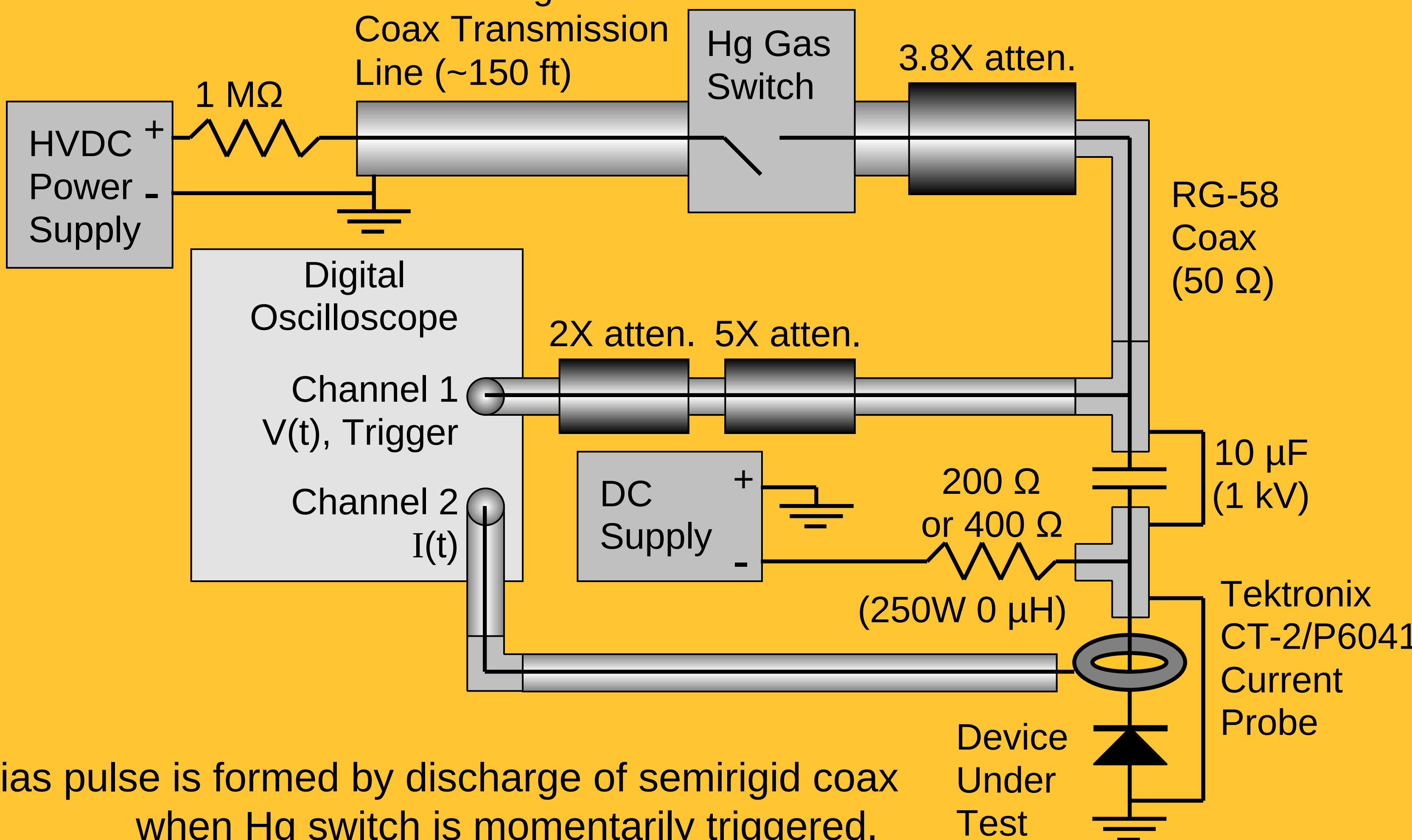
- Stable and unstable SiC reverse breakdown.

Forward bias diode pulse testing

- Rectifier reverse recovery switching transients.
- Perimeter-governed device minority carrier lifetimes.

These behaviors directly impact SiC power device performance & reliability.

Pulse Test Circuit



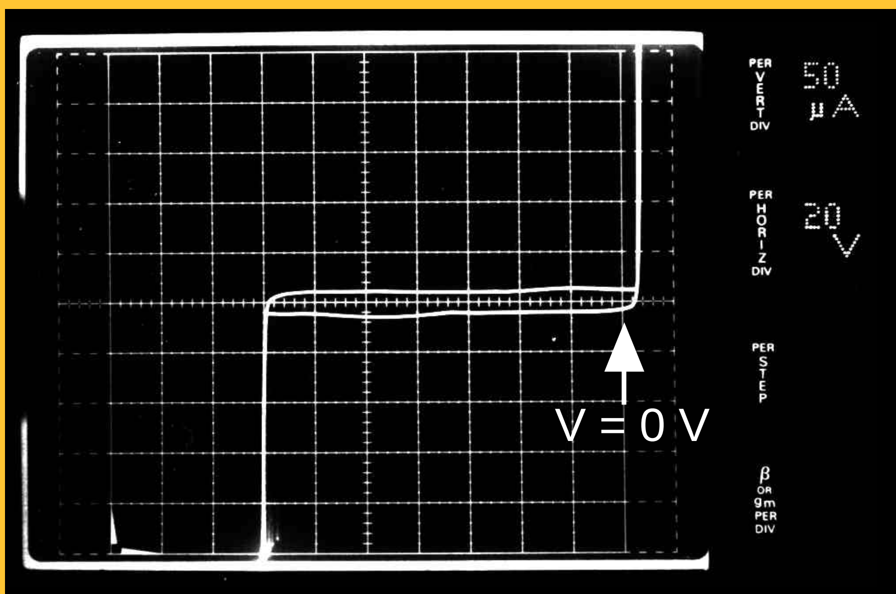
Bias pulse is formed by discharge of semirigid coax
when Hg switch is momentarily triggered.

A Tale of Two Diodes

(Part 1: DC Testing)

Epitaxial Small-Area 4H-SiC $p^{+}n$ Diodes

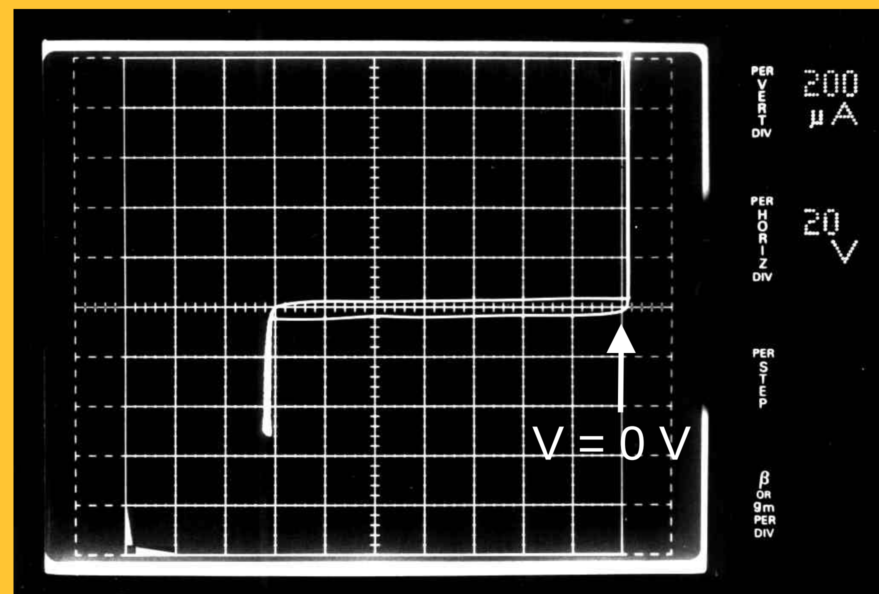
Wafer A*



$V_{DC\ BKDN}$ = 140 V

* NASA Lewis Run #1841
J. Appl. Phys. **80**, p. 1219

Wafer B**



$V_{DC\ BKDN}$ = 142 V

** NASA Lewis Run #1905
IEEE EDL **18**, p. 96

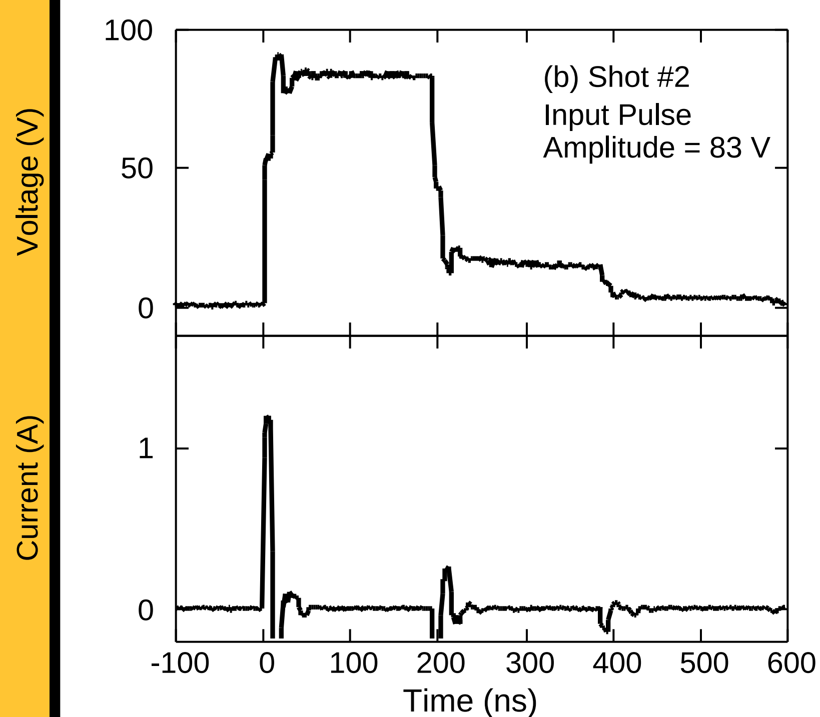
A Tale of Two Diodes

(Part 2: Reverse Bias Pulse Testing)

Experiment: Subject devices to single-shot reverse-bias pulses of increasing amplitude until catastrophic breakdown failure occurs.

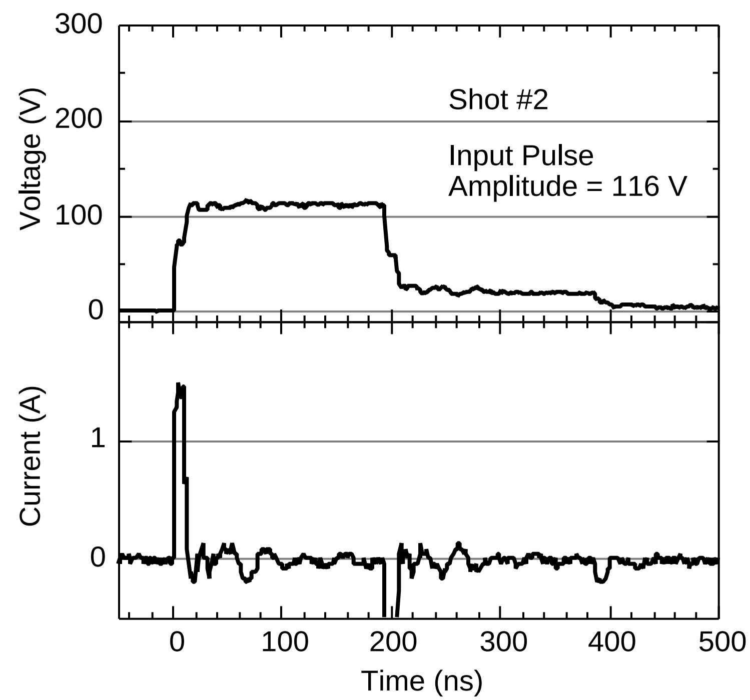
Wafer A

($V_{DC\ BKDN}$ = 140 V)



Wafer B

($V_{DC\ BKDN}$ = 142 V)



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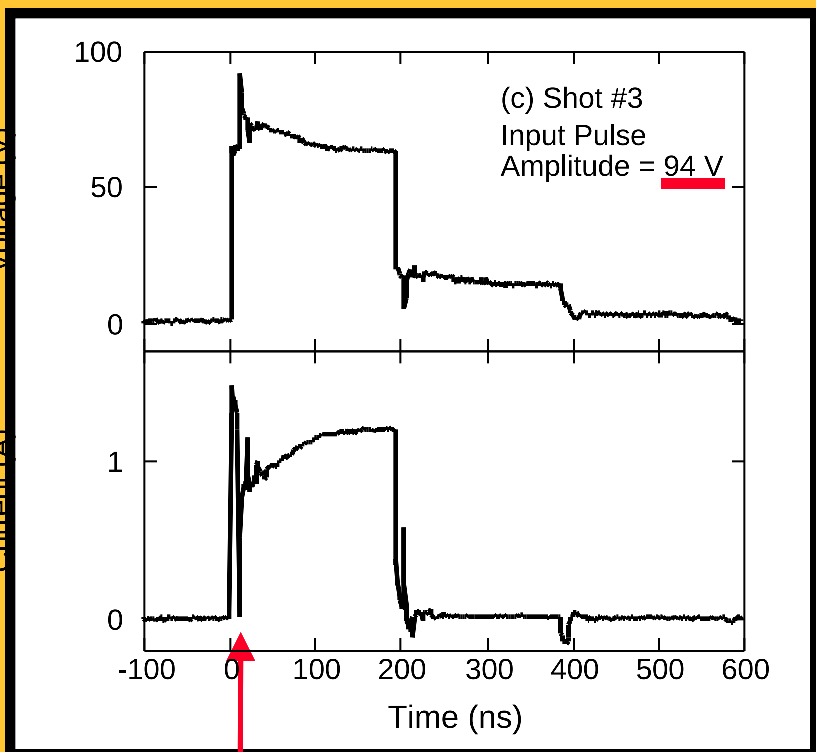
**INSTRUMENTATION & CONTROL
TECHNOLOGY DIVISION**

A Tale of Two Diodes

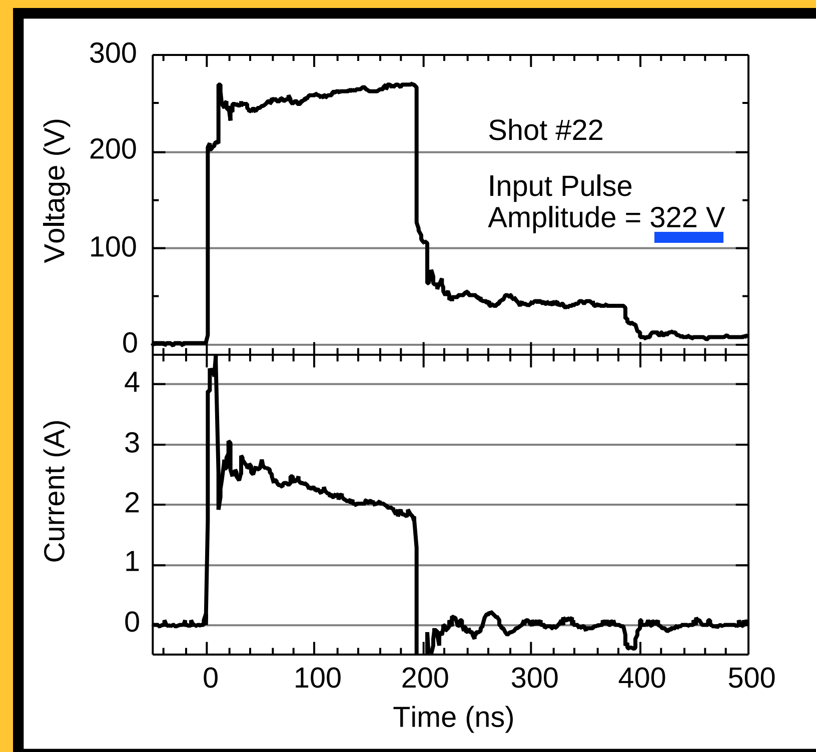
(Part 2: Reverse Bias Pulse Testing)

Wafer A
($V_{DC\ BKDN}$ = 140 V)



Catastrophic Device Failure,
Device Physically Destroyed!

Wafer B
($V_{DC\ BKDN}$ = 142 V)



Device Still Good,
Positive Temp. Coeff. Breakdown!

PGN9/97

Pulse Breakdown Discussion

Behavior of devices on Wafer A is unacceptable for many power applications.

- Extremely high reliability, immunity to "glitches" required for most aerospace applications.

Differences between "unstable" Wafer A and "stable" Wafer B:

- Single epi-growth (Wafer B) vs. two-step epi growth (Wafer A).
- SIMS revealed excess Al, N near Wafer A junction not present in Wafer B.
- n-substrate (Wafer B) vs. p-substrate (Wafer A).

Exact physical mechanism still uncertain.

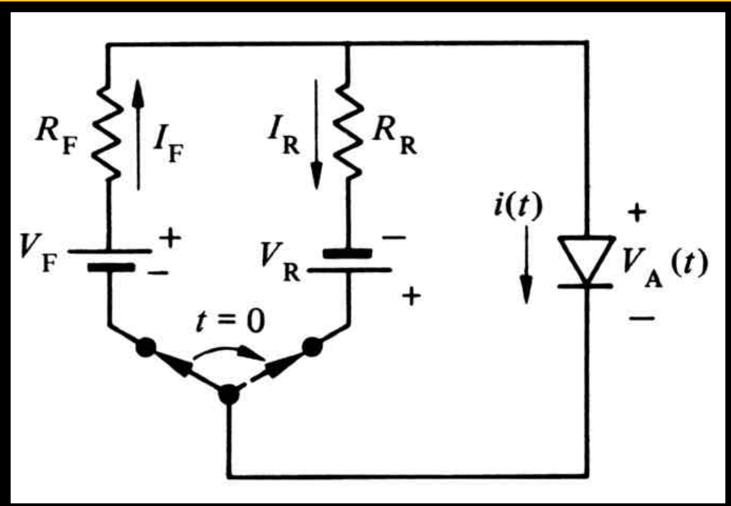
- Bulk failure mechanism - <u>no evidence of surface breakdown.</u>

Positive temperature coefficient breakdown observed only on very small-area ($A < 1 \times 10^{-4}$ cm^2) Wafer B devices.

- Elementary (1c) screw dislocations affecting breakdown???

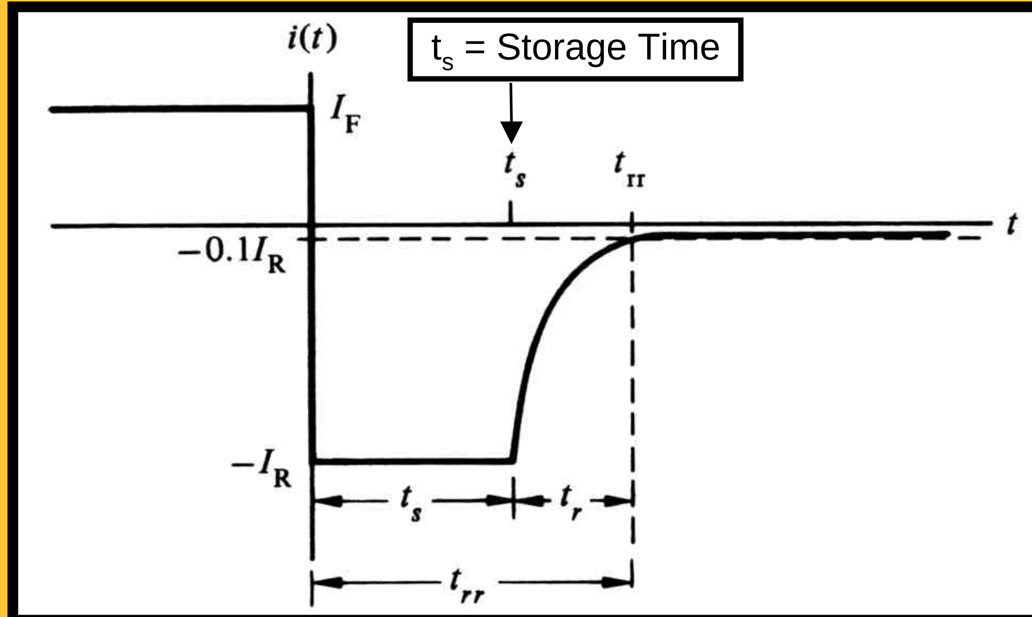
PN Diode Reverse Recovery*

Idealized Test Circuit



(zero inductance)

Diode Reverse Recovery Current Transient



Minority carrier (hole) lifetime τ_p
related to storage time t_s by:

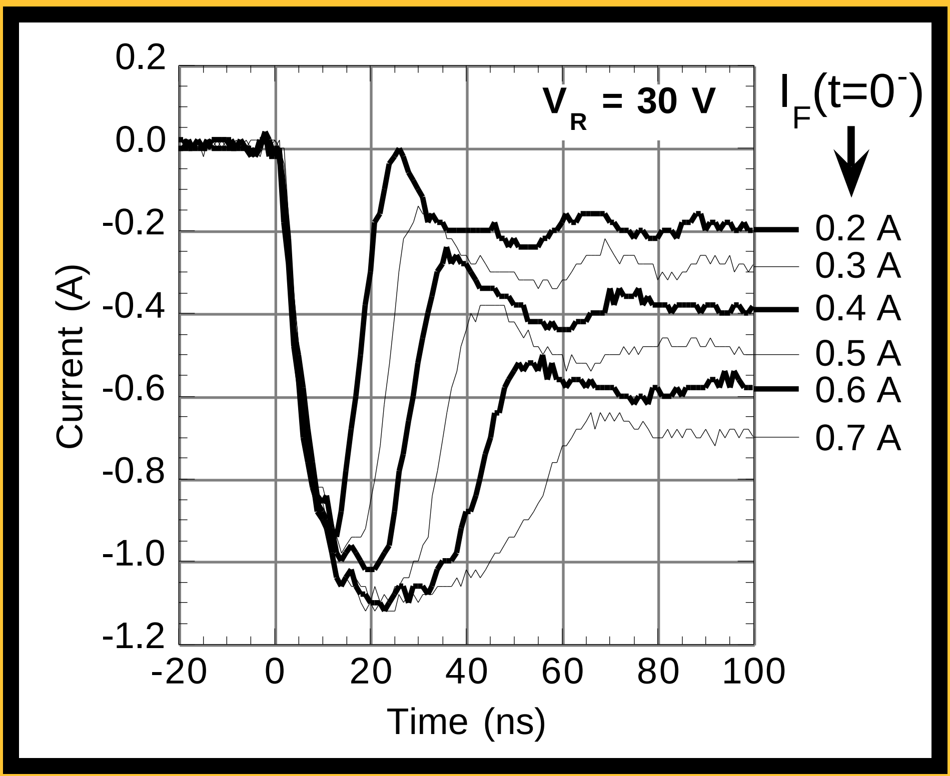
$$t_s = \tau_p \left\{ \mathrm{erf}^{-1}\left[1 + \frac{1}{I_R / I_F} \right] \right\}^2$$

* G. Neudeck, The PN Junction Diode, 2nd Ed., Addison-Wesley Publishing, p. 111.

Reverse Recovery Current Transients

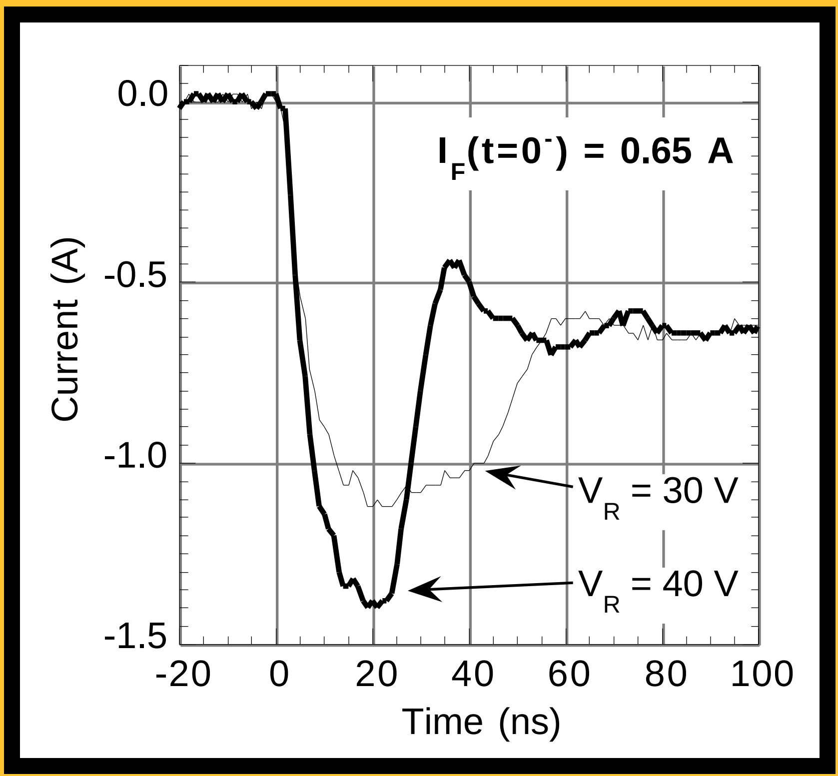
Device Area = 8.1×10^{-3} cm^2, R_s = 200 Ω

I_F varied for approximately fixed I_R



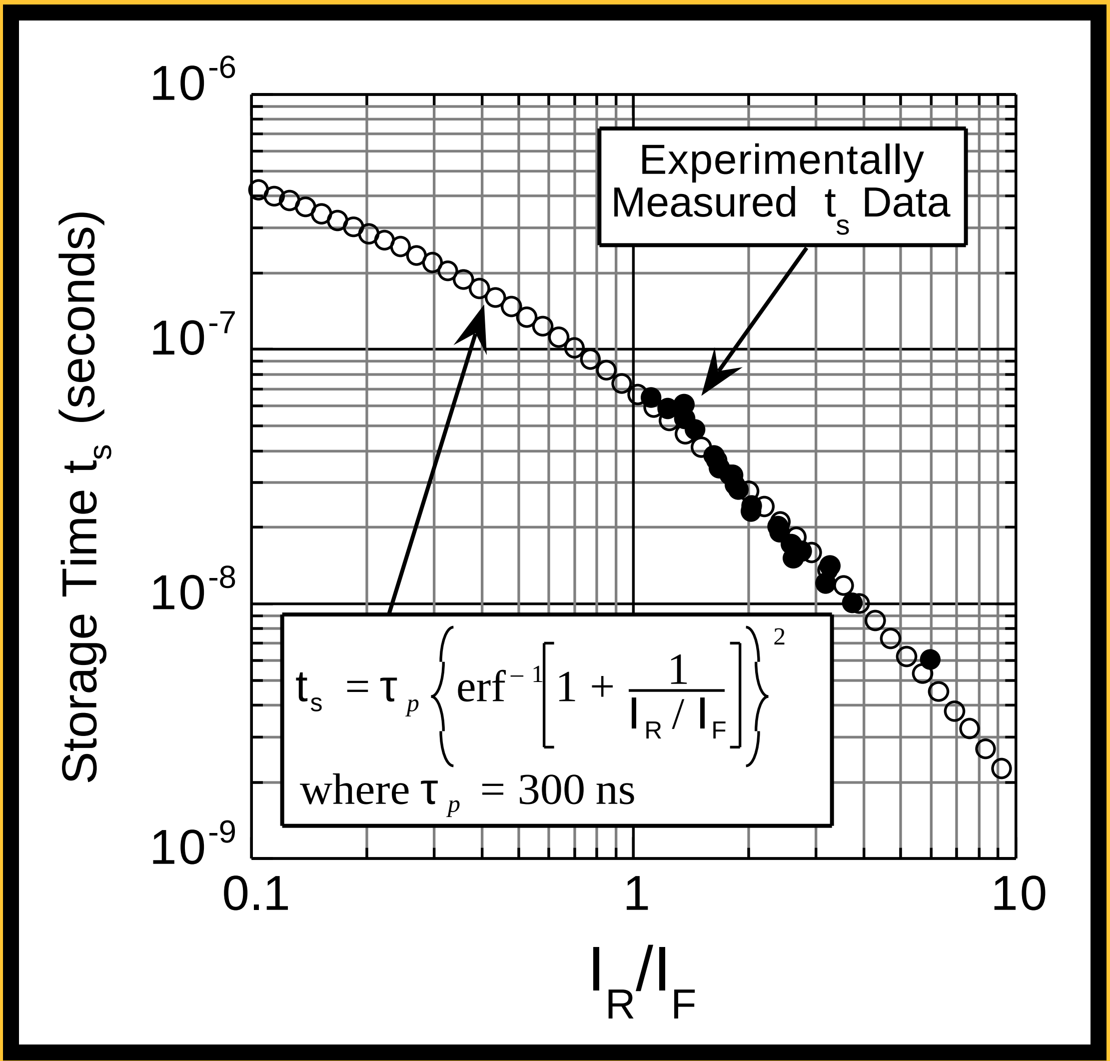
t_s increases as I_F increases.

I_R varied for fixed I_F



t_s decreases as I_R increases.

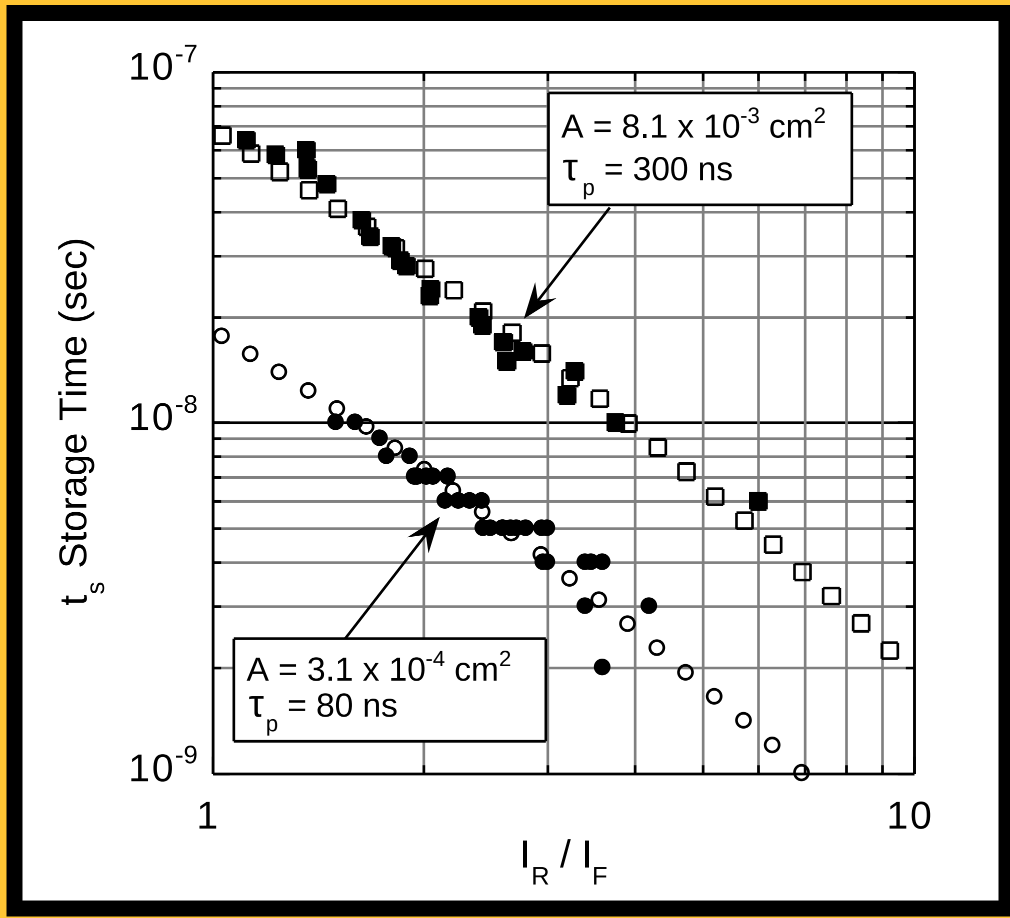
Storage Time (t_s) Dependence on I_R/I_F



Experimentally measured storage time behavior follows predicted physical theory.

Effective minority carrier lifetime for this device is 300 ns (A = 8.1 x 10^{-3} cm^2)

Storage Times (t_s) of Larger vs. Smaller Devices

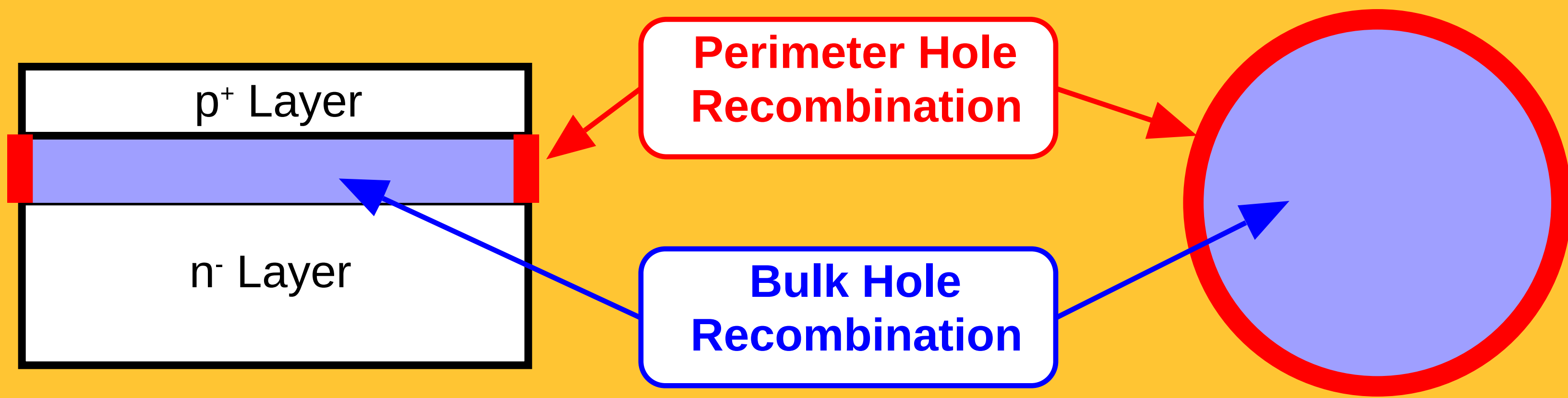


Effective minority carrier lifetime decrease with decreasing area suggests presence of significant perimeter surface recombination effects.

p^+n Diode Effective Lifetime

Side View of Diode

Top View of Diode



Device Hole Recombination = $R_{Eff.}A = R_{Bulk}A + R_{Perim.}P$

$\tau_{p\,Eff.} = \tau_p$ extracted from reverse recovery switching measurement t_s vs. I_R/I_F data.

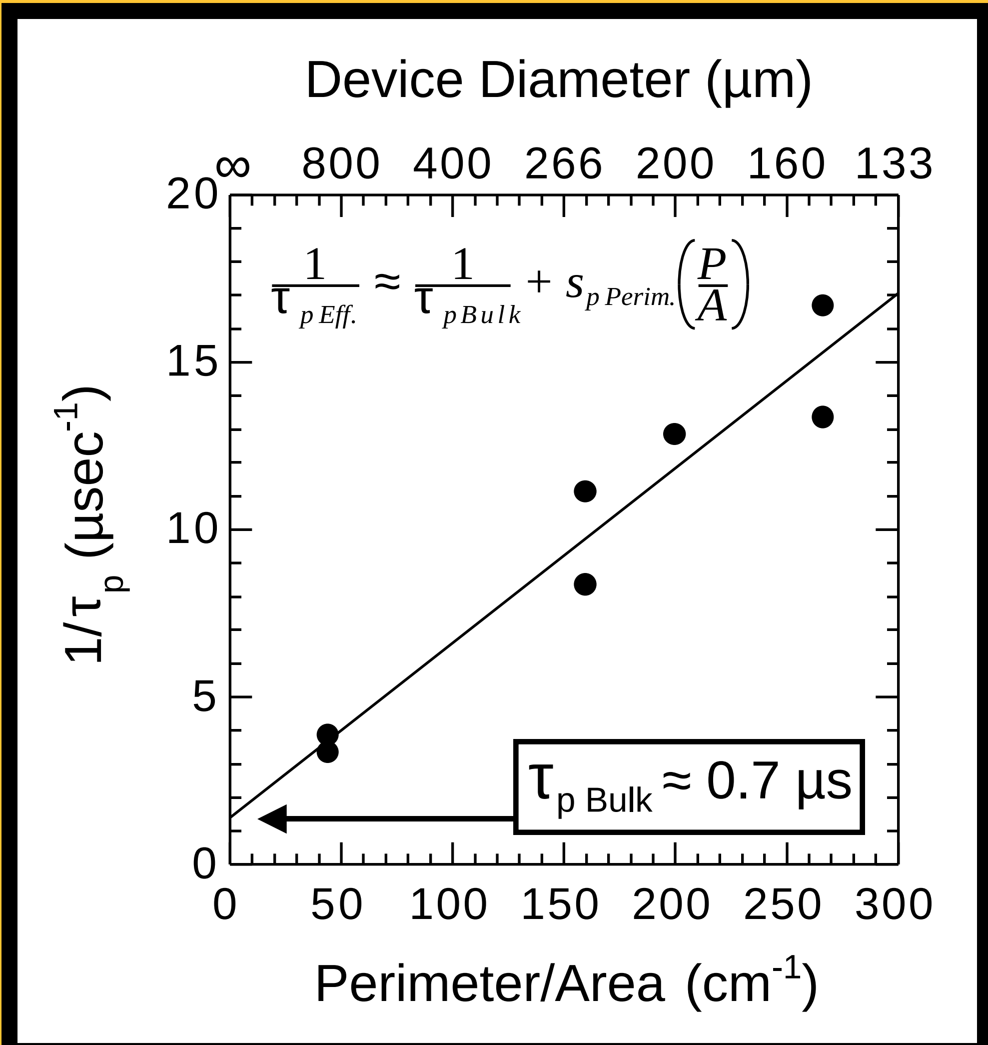
$$\frac{\Delta p_n}{\tau_{p\,Eff.}} A \approx \frac{\Delta p_n}{\tau_{p\,Bulk}} A + s_{p\,Perim.} \Delta p_n P$$

$$\frac{1}{\tau_{p\,Eff.}} \approx \frac{1}{\tau_{p\,Bulk}} + s_{p\,Perim.}\left(\frac{P}{A}\right)$$

$$y = b + mx$$

Can estimate $\tau_{p\,Bulk}$ and $s_{p\,Perim.}$ from linear plot of $1/\tau_{p\,Eff.}$ vs. P/A.

Bulk Minority Carrier Lifetime Extraction



$$\frac{1}{\tau_{p\,Eff.}} \approx \frac{1}{\tau_{p\,Bulk}} + s_{p\,Perim.}\left(\frac{P}{A}\right)$$

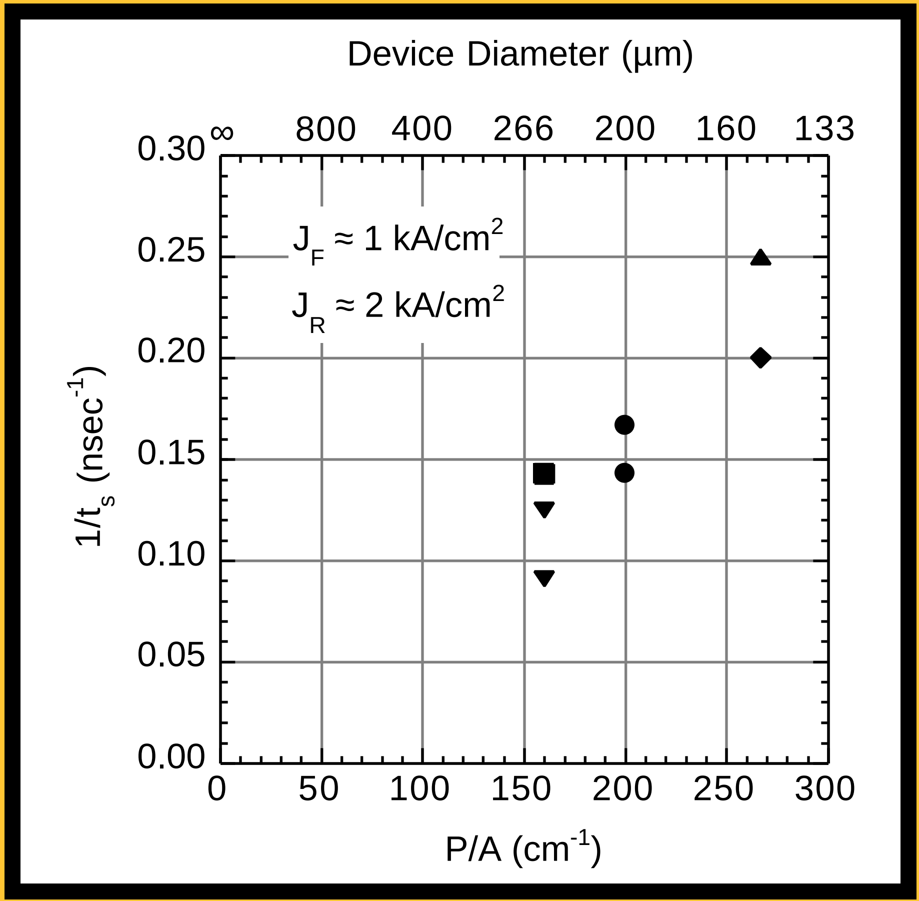
$$y = b + mx$$

$\tau_{p\ \mathrm{Bulk}} \approx 0.7\ \mu s$

(4H-SiC, $N_D = 2 - 4 \times 10^{16}\ cm^{-3}$)

The **bulk** minority carrier lifetime inherent to this SiC epilayer is much longer than the **average** lifetime measured on a small-area device. This is due to large perimeter surface recombination.

Storage Times at Constant Current Density



Indicates bulk Auger recombination insignificant compared to perimeter-governed SRH recombination.

Discussion

This work demonstrates by example that perimeter surface recombination can significantly impact SiC bipolar device electrical characteristics via reduced effective minority carrier lifetimes.

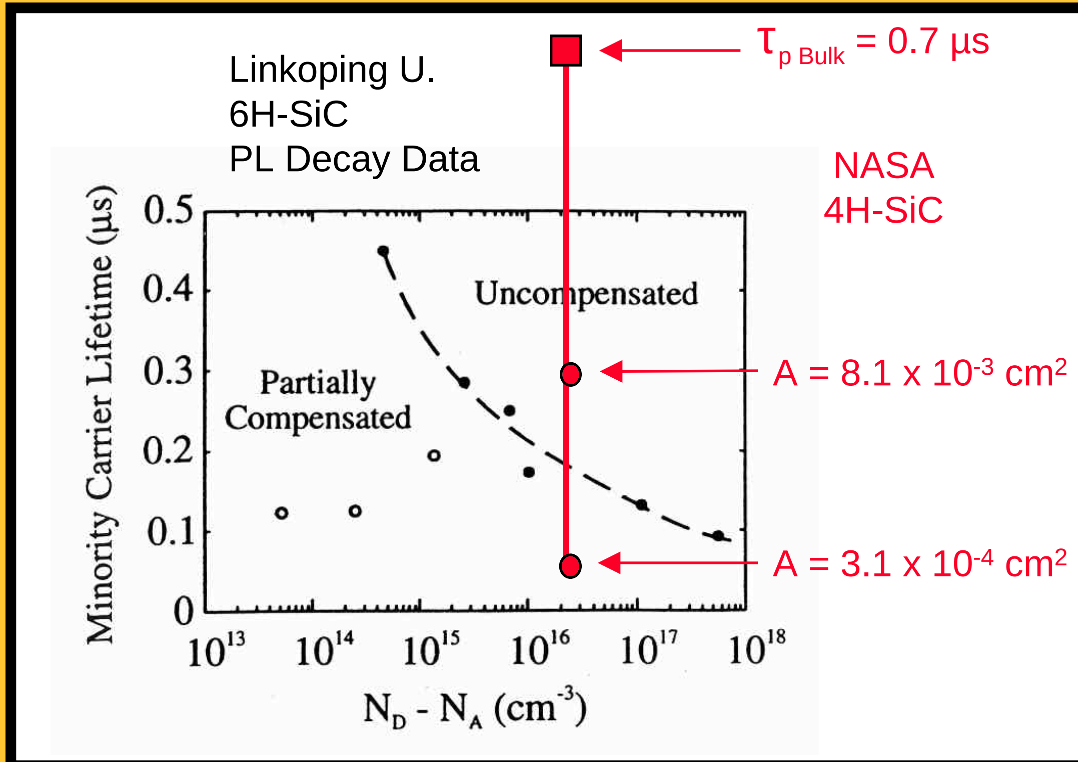
- Possible contributing factor to experimental observations of:
  - Low current gains (< 20) in SiC BJT's produced to date.
  - SiC pn diode current densities below theoretical predictions.
  - Fast switching response of SiC pn diodes and thyristors.
- Greater impact on smaller (IC) devices than larger (power) devices.
- Lifetime reduction likely to be exacerbated by "multi-finger" or "multi-cell" geometries that increase effective perimeter-to-area ratio.

Development and optimization of appropriate SiC surface passivation and junction termination technologies could reduce or eliminate lifetime-limiting role of surface recombination in SiC bipolar devices.

Discussion (cont.)

- Potential impact on n- or p-type 4H- and 6H-SiC at all doping densities (?).

Figure from
Janzen & Kordina,
ICSCRM-95 p. 657.



- Effect present in ion implanted or heavily compensated SiC junctions?

Summary

Pulse testing reveals very important device behaviors not observed by conventional DC and RF testing.

Observed behaviors directly impact SiC power device

- reliability
- switching speed
- current (density) rating

Pulse testing should play an important role in SiC power device development and qualification.